Single-Chip Direct Digital Synthesis (DDS) versus the Analog PLL

- *Complete-DDS chips with DAC have excellent AC performance, low power & price, small size*

by Jim Surber and Leo McHugh

- **New integrated Complete DDS products present an attractive alternative to analog PLLs for agile frequency synthesis applications. Direct digital synthesis (DDS) has long been recognized as a superior technology for generating highly accurate, and frequency-agile (rapidly changeable frequency over a wide range), low-distortion output waveforms. DDS architecture** (**Figure 1**) **employs a precision phase accumulator and digital signal-processing techniques to generate a digital sine wave representation which is referenced to a highly-stable reference clock.** The digital sine-wave data is then applied to a high-speed Digital to Analog Converter (DAC) to generate a corresponding analog sinewave output signal.

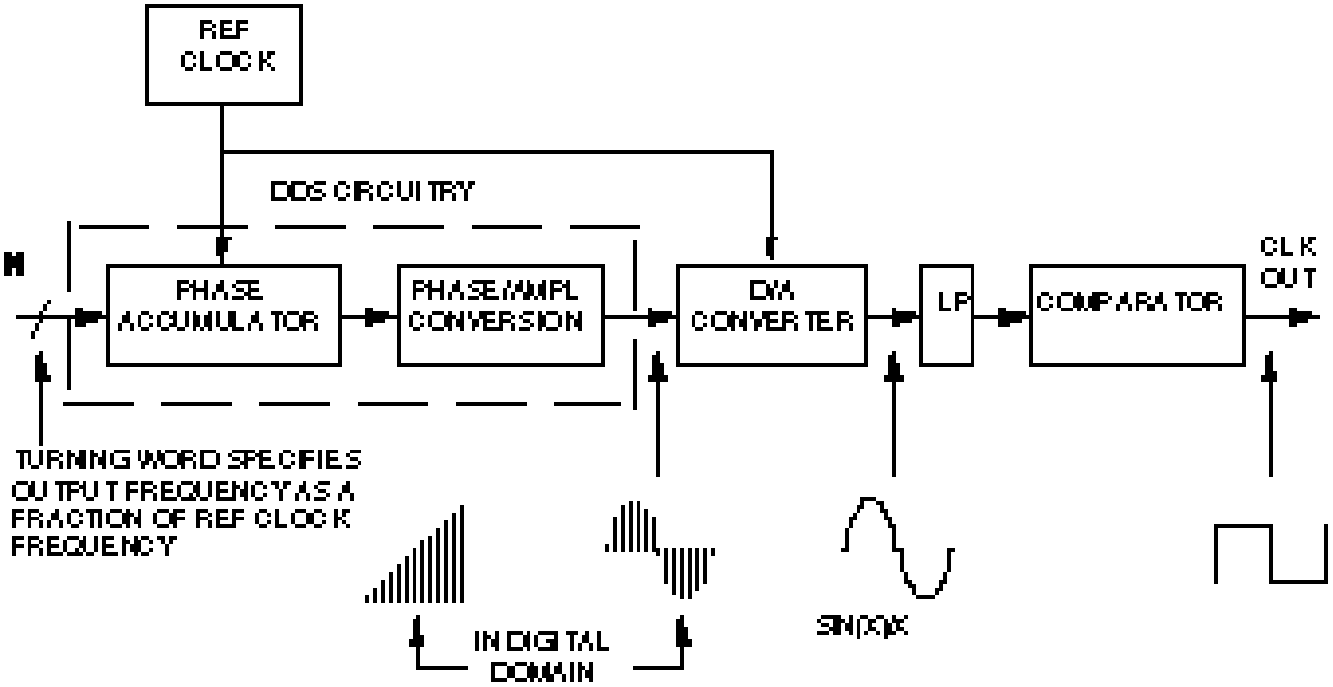

Figure 1. Basic Complete-DDS system block diagram.

A major advantage of a DDS system is that its output frequency and phase can be precisely and rapidly manipulated under digital processor control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution (frequency control in the millihertz (mHz) range and phase control < 0.09°, and to rapidly "hop" in frequency (up to 23 million output frequency changes per second). These characteristics have combined to make the technology extremely popular in military radar and communications systems. In fact, DDS technology was previously relegated almost exclusively to high-end and military applications: it was costly, power-hungry (dissipations specified in *watts*), difficult to implement, required a discrete high-speed signal DAC, and had a set of user-hostile system interface requirements.

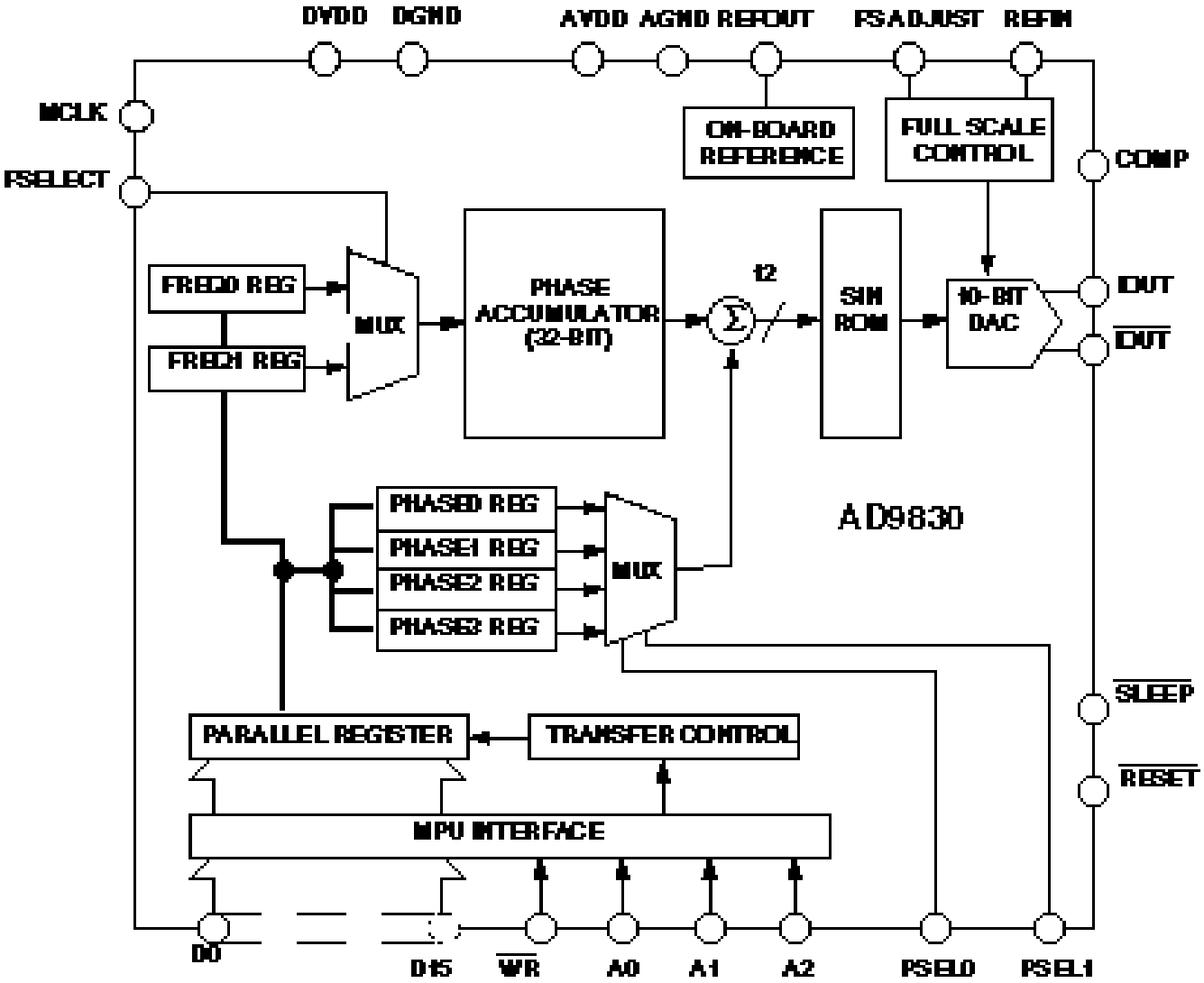

***Figure 2**. **Block diagram of AD9830 50-MHz C-DDS**.*

A new family of breakthrough CMOS digital synthesizer products from Analog Devices increases the attractiveness of DDS-based synthesizer solutions. The AD9850 (125-MHz) and AD9830 (50 MHz) *Complete*-DDS (CDDS) devices include on-chip 10-bit signal DACs (**Figures 2 and 3**). They are optimized for low output distortion, with spurious-free dynamic range (SFDR) of 72 dBc narrowband and up to 54 dBc wideband @ 40 MHz. Additional product features, such as small surface-mount packaging, extremely low power dissipation (as low as 155 mW at +3.3 V), increased functionality, and low price, combine to ensure that these devices are indeed the State-of-the Art in DDS technology. They now permit users to address cost-sensitive, high-volume, consumer synthesizer applications; and **they present a viable alternative to analog-based Phase-Locked Loop (PLL) technology for generating agile analog output frequency**. The AD98x0 devices should be uniquely attractive for local oscillator (LO) and up/down frequency conversion stages-which were until now the exclusive domain of PLL-based analog synthesizers. The Complete-DDS architecture of the AD98x0 devices holds distinct advantages over an equivalent PLL-based agile analog synthesizer for many reasons. For example: **Output frequency resolution: the AD98x0 C-DDS products have 32-bit phase accumulators, which enable output frequency tuning resolutions much finer than a PLL-based synthesizer can enjoy**. The AD9850 has a tunable output resolution of 0.06 Hz, with a clock frequency of 125 MHz; the AD9830 has a tuning resolution of 0.012 Hz, with a reference clock of 50 MHz. Furthermore, the output of these devices is phase-continuous during the transition to the new frequency. In contrast, the basic PLL-based analog synthesizer typically has an output tuning resolution of *1 kilohertz*; it lacks the inherent resolution afforded by the digital signal processing. Output-frequency switching time: the analog PLL frequency switching time is a function of its feedback loop settling time and VCO response time, typically > 1 ms. C-DDS-based synthesizer

switching time is limited only by DDS digital processing delay; the AD9850's minimum output frequency switching time is 43 ns. Tuning range: A critical feedback loop bandwidth and input reference frequency relationship determines the stable (usable) frequency range of the typical analog PLL circuit. C-DDS-based synthesizers are immune to such loop filter stability issues and are tunable over the full Nyquist range (< 1/2 the clock rate). Phase noise: Because of the frequency division, C-DDS-based solutions have a clear advantage over analog PLL synthesizers in output phase-noise. The output phase noise of a C-DDS synthesizer is actually better than that of its reference clock source, while analog PLL-based synthesizers have the disadvantage of actually multiplying the phase noise present in their frequency reference. Board-space requirement: The highly integrated AD98x0 C-DDS devices are packaged in very small surface-mount packages requiring no more board space than most high-quality equivalent-bandwidth discrete PLL synthesizer implementations. Cost: Shattering existing DDS price barriers, C-DDS-based solutions are competitive in high-volume applications with bandwidth-equivalent discrete PLL-based synthesizer solutions. Power-dissipation: C-DDS synthesizers dissipate much less power than earlier discrete DDS solutions. For example, the AD9850 dissipates 155 mW at 3.3 V when generating a 40-MHz signal, with a 100 MHz reference clock. This is competitive with comparable discrete analog PLL circuits. Implementation complexity: Complete-DDS solutions, which include the signal DAC, translate to ease of system design. There is no longer an element of RF design expertise required to implement a DDS solution; the hard part has been done. A simple digital instruction set for control minimizes the complexity of support hardware. Digital system design replaces the analog-intensive system design required for PLL-based analog synthesizer solutions to similar problems.

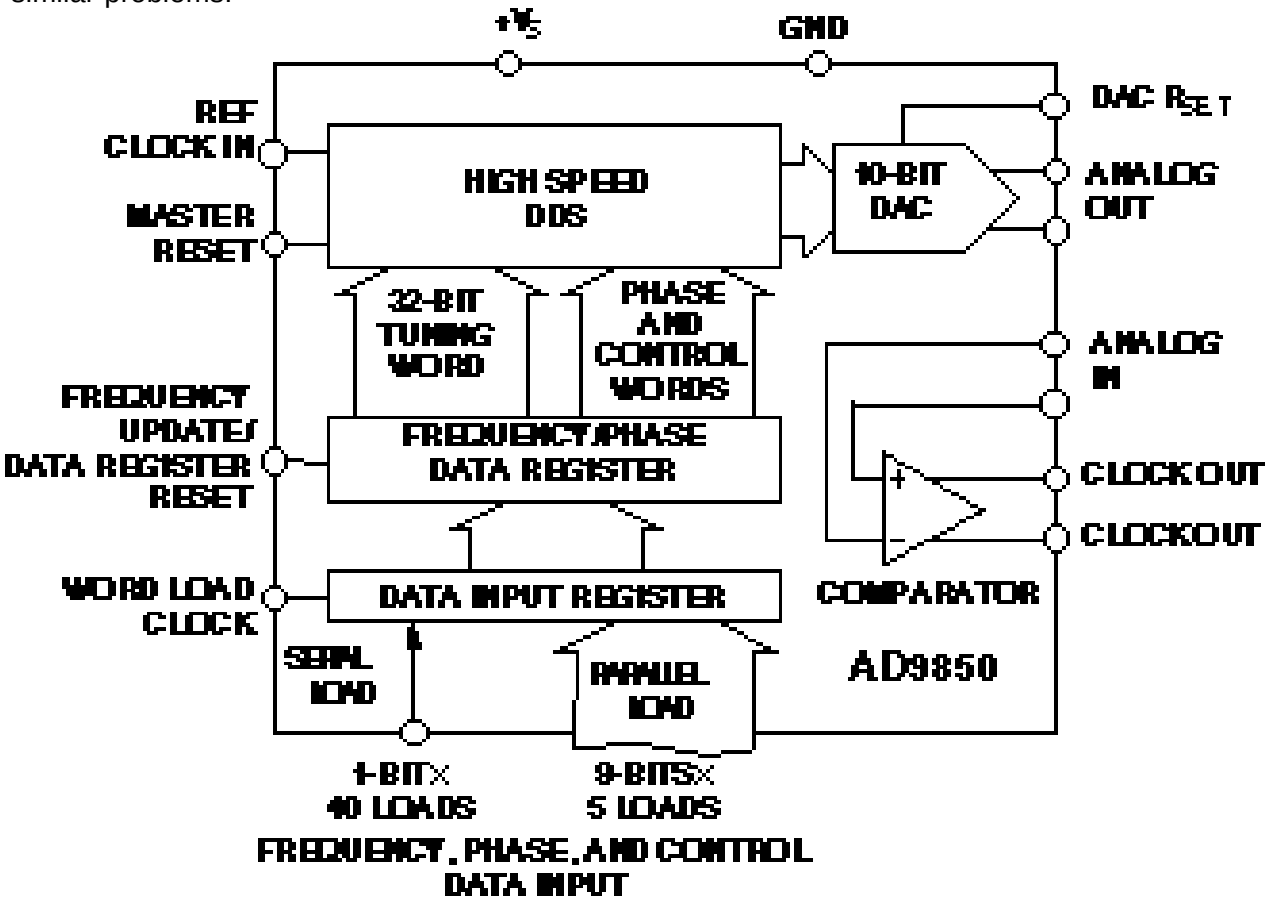

***Figure 3**. **Block diagram of AD9850 125 MHz C-DDS**.*

AC performance is an important consideration in the choice of a frequency synthesizer. The distortion performance of a C-DDS synthesizer system is limited by its signal DAC; and the AD98x0 devices set a new benchmark in CMOS DAC performance. Their on-board 10-bit DAC cores have been intensively optimized for high SFDR over wide output bandwidths, and are technological breakthroughs in their own right (see pages 7-9 of this issue). Figures 4 and 5 show wideband spectral plots of the output of the AD9850 generating 5-MHz and 40-MHz output

frequencies with a 125-MHz reference clock. The demonstrated SFDR of the output of the AD9850 is 62.8 dB and 55.2 dB (respectively) over the 62.5 MHz Nyquist bandwidth (1/2 the reference clock rate). Such dynamic performance was previously achievable only with expensive bipolar DACs dissipating several watts.

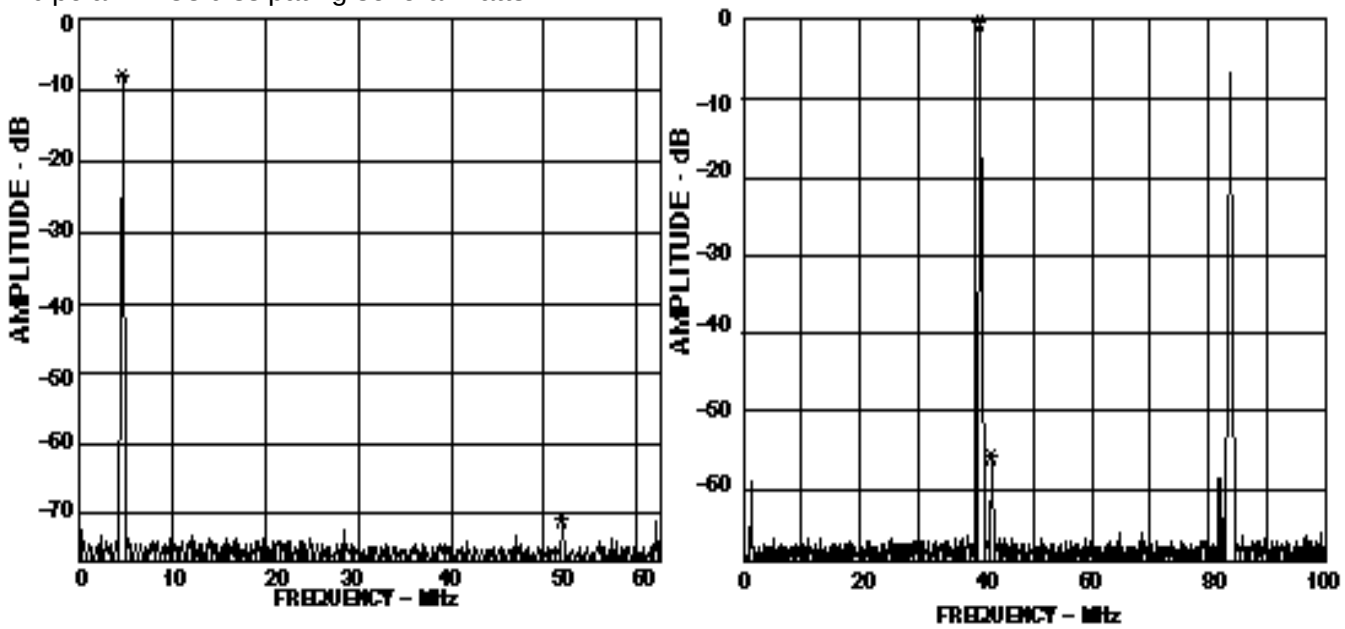

Figure 4. AD9850 wideband spectral plot at 5 MHz Aout (125-MHz clock).

Figure 5. AD9850 wideband spectral plot at 40 MHz Aout (125-MHz clock).

In other applications, many of them dominated by analog PLL-based synthesizer solutions, *narrowband* performance is an important consideration. In narrowband applications the spur performance of the C-DDS synthesizer's output is largely gated by the digital truncation level of the DDS rather than DAC's performance. Figure 6 shows a narrowband plot of the AD9830 at 4.16-MHz A_{out} and a 50-MHz clock. The SFDR is shown to be greater than 79 dB over a ±5 kHz window of the fundamental.

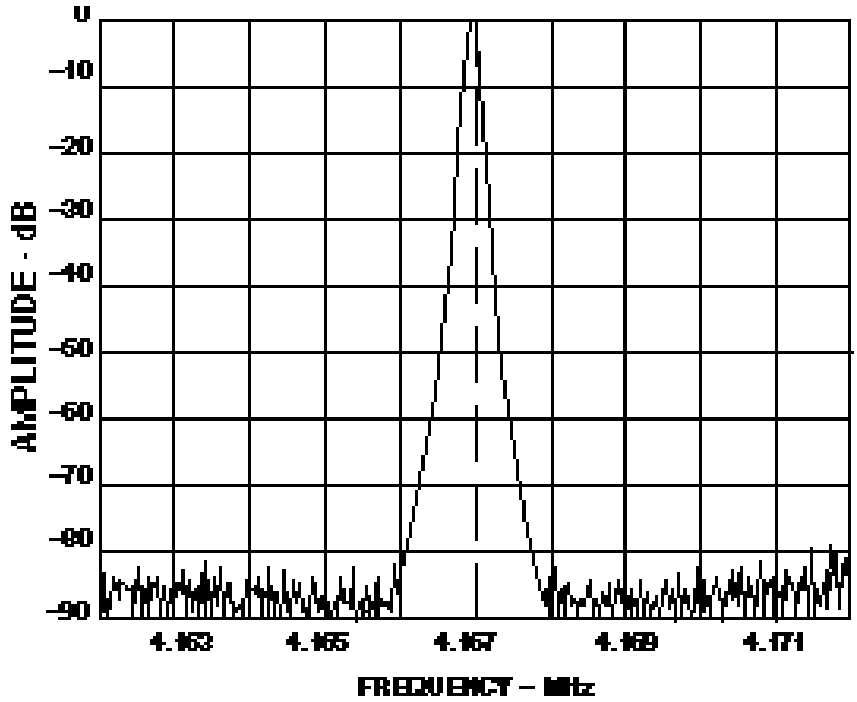

Figure 6. AD9830 narrowband spectral plot 4.1 MHz Aout (50 MHz clock).

Both the AD9850 and the AD9830 utilize a very simple loading scheme for user-friendly operation. They require only a data clock and data/address bus to control the output frequency and phase and to enable the sleep mode. No analog-intensive system design is required, except

for the specific requirements of output filtering. The AD9850 has a useful additional feature: an integrated high-speed comparator. The filtered output of the DAC can be applied to this comparator to generate a square wave out instead of a sinewave, facilitating the use of the device as a frequency-agile clock generator. PC-compatible evaluation boards are available for both devices to facilitate bench testing of the synthesis system. **The combination of fast output hopping, digital control, low output distortion, and high tuning resolution makes the Complete-DDS solution a viable alternative to analog PLL synthesizers.** The AD9830 and AD9850 breakthroughs in CMOS DAC and DDS technology warrant serious consideration for any frequency synthesizer requirement. ***The AD9830 was designed in Limerick, Ireland, by Hans Tucholski****, and* ***the AD9850 was designed in Greensboro, NC, by Dave Crook and Tim Stroud***

Feature/Specification	**AD9850**	**AD9830**
Maximum clock frequency	125 MHz	50 MHz
Maximum output Nyquist-frequency bandwidth	62.5 MHz	25 MHz
Frequency tuning word resolution	32 bits	32 bits
Phase tuning word resolution	5 bits	12 bits
Supply voltage	+3.3 V / +5 V	+5 V
Power dissipation @ max. operating conditions	155 / 380 mW	265 mW
Worst-case narrowband SFDR (±50-kHz window) @ max. clock	72 dBc	72 dBc
Wideband SFDR (Nyquist) @ 20-MHz Aout	58 dBc	50 dBc
Wideband SFDR (Nyquist) @ 40-MHz Aout	54 dBc	N/A
Control interface	Parallel / serial	Parallel
Unique additional features	Internal high-speed comparator registers	Two frequency four phase registers
Package style	28-pin SSOP	48-pin TQFP
Price	$14.55	$11.70
Faxcode	1990	1993