RADIO DESIGN FOR FUTURE WIRELESS SOC PLATFORMS: AN OVERVIEW

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ABSTRACT

As we move to third and fourth generation wireless providing higher data rates at shorter distances in "hotspots", future handhelds will be able to access different wireless infrastructures, e.g. UMTS and WLAN, from the same wireless device, be it a mobile phone, a PDA or a notebook. As a result SoC platforms for convergent 4G must address the challenge of increased complexity particularly as it pertains to the radio transceiver part of a chipset where power consumption and cost are the main differentiators.

This paper presents an overview of the challenges faced in designing highly integrated radios in the context of 4G wireless communications. Aside from important issues such as multi antenna design and standards coexistence in the same SoC platform, we focus our overview on a few main thrusts that will be discussed in some details related to designing digitally programmable and configurable ADCs, PLLs, analog baseband chains and RF front ends as well as techniques for packaging multi band radios and for achieving "first pass" silicon success.

1. INTRODUCTION

The rapid progress of integrated circuit (IC) technology and continuous down-scaling of CMOS technology has benefited digital technology and was the main driver behind the shift from analog modulation techniques to digital ones while migrating from first to second and future wireless generations. On the other hand, the analog and RF technology continues to present a major challenge for a true fully integrated solution. For example, to achieve higher data rates in emerging wireless generations, such as WCDMA and IEEE 802.11g, the analog front-end must be able to handle wider bandwidths at lower noise and power levels. Current and future trends, see Figure 1, call for designs at very small feature sizes, 0.13 micron and smaller, at supply voltages of 1V and smaller. Under these conditions, random process variations become very severe causing further degradation of analog and RF performance.

Furthermore, analog, mixed-signal and RF design, which follows a complex procedure of optimisation and trade-offs between many design parameters, is still lagging in design automation, takes longer time to design and may require several silicon spins. These challenges must be perceived as opportunities for innovative solutions targeting digitally programmable and reconfigurable design solutions for multistandard convergent wireless applications, see e.g. Refs. [1]–[6].

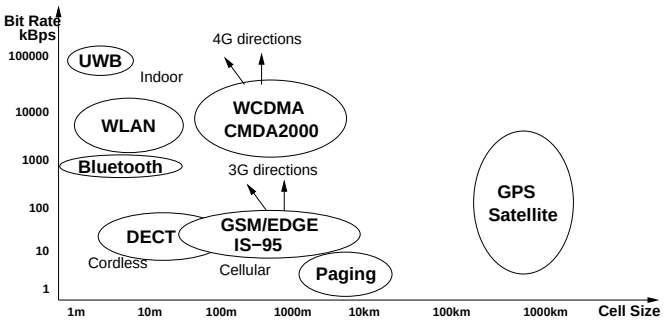

Fig. 1. Wireless Standards Roadmap

A wireless chipset normally contains a radio chip, a digital baseband chip and a power amplifier. While successful efforts have recently been made to develop highly integrated multistandard digital baseband chips, existing wireless devices mostly use "stacked" radio transceivers, i.e. separate transceivers for different standards. This represents a major bottleneck in attempting to achieve a higher level of integration and in reducing the bill of materials for the total wireless solution towards reaching the ultimate goal of maximising the performance-to-cost ratio.

Towards that end, new design methodologies should aim to achieve a small form factor, low-power low-voltage, robust, manufacturable design that can be completed in a short time. To reach these objectives, research efforts should fo-

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cus on innovative analog front-ends that are characterised by the following:

* Architectures suitable for monolithic integration and first-pass silicon,

* Designs based on regular modules for maximum reuse, maximum hardware share and shorter design time,

* Multistandard support with configurable radios and programmable mixed-signal basebands to accommodate different channel bandwidths and data rates,

* Digitally programmable structures to simplify the interface with the DSP and allow for an optimum mixed-signal system solution,

* Digital correction and calibration of analog-, mixed-signal- and RF-blocks.

* Robust designs adopting yield enhancement and incorporating random process and digital interference variations into the proposed methodology.

* Investigation of and finding the best trade-offs for on-chip vs off-chip packaging for multistandard solutions.

2. VISION AND GOALS

Software Defined Radio (SDR) is a conceptual radio design where functions may be defined in software (e.g. by downloads or subscriber identity cards). This can also be viewed in the context of wireless convergence. As such, an ideal SDR is a multiband, multicarrier and multistandard radio with dynamic capability defined through software in all layers of the protocol stack, including the physical layer. Achieving such dynamic capability of the physical layer of a SDR, in particular the radio transceiver, is one of the main trends going forward.

Another aspect to our vision is to exploit digital solutions to analog problems towards the ultimate goal of achieving first-pass silicon for designs in very small feature sizes and at very low supply voltages of 1 V and below. When migrating to smaller feature sizes, digital calibration, correction and programmability techniques will be used to offset and correct for performance degradation of analog and RF parts. Such degradations become very severe with increased random process variations associated to smaller feature sizes. The digital silicon area overhead used to restore analog and RF performance will be kept to a minimum as digital technologies follow Moore's law, resulting in high-performance cost-effective radio solutions for future convergent wireless applications.

3. FUTURE DIRECTIONS

The different standards operating in the frequency range of up to 6 GHz, with even higher frequencies with the introduction of Ultra Wide-Band (UWB) techniques, arises the need and gives a key role to multistandard RF transceivers which combine several cellular and cordless phone standards as well as wireless LAN functionalities in one unit.

Based on this fact, future directions will target areas of high strategic interest to the wireless and mobile community during the coming decade organised in 6 main thrusts, namely, architectures for and analysis of multiband radios, RF-front ends, techniques for robust design, programmable bandwidth frequency synthesisers, programmable and configurable baseband chains and programmable data converters for multiband and multistandard operation. The resulting new design methodology should aim to offer innovative design solutions within these areas in the context of issues of software configurability, robustness, low-voltage operation and the impact of technology scaling, see e.g. Ref. [7].

A conceptual sketch visualising the different thrusts is shown in Figure 2. At the architectural level analysis techniques and design approaches which are adaptable to multistandard wireless systems should be explored.

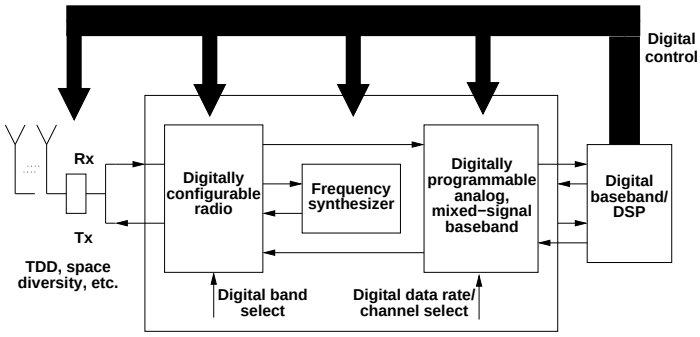

Fig. 2. A block diagram for a programmable radio.

Below we discuss the main thrusts in some detail.

3.1. Architectures for and analysis of multiband radios

We propose to develop a suite of architectural analysis techniques and design approaches that are especially adaptable to multistandard wireless systems. Analysing a multistandard system requires particular attention to be paid to architectural design. At the top level, choice of architectures is characterised by the need to operate the same hardware across multiple frequency bands requiring careful frequency planning for interference rejection. Technology scaling which actually dictates low supply voltages, will have a strong impact to sampling strategies and structures influencing the overall down-conversion strategy.

One solution would be to bring in the advantages of digital technology by applying self calibration and correction techniques and use adaptive DSPs. These digital techniques could be used for receivers, LNAs, etc. This will also contribute to our aim of first-pass design success, by monitoring the performance achieved and applying on-line digital cor-

rection in order to reach the performance goals while minimising silicon spins.

Classical heterodyne, zero-IF, low-IF and wideband-IF need to be complemented with new conversion schemes. The extent to which hardware sharing can be used is determined by limitations on wideband circuit design. Trade-offs between bandwidth, noise figure, linearity, and power consumption must be addressed with a modelling toolbox suited for multistandard analysis.

From the bottom-up, a mechanism to feed chip test results into the block-level design should be developed. Such an approach allows iterative enhancement in multistandard performance, and also helps us to optimise against various design trade-offs at the system level with the goal of optimising both the system and the individual blocks. Since working in the deep submicron region causes severe degradation in analog and RF circuit performance, solutions to overcome this problem need to be offered.

Efforts to find solutions for fist-pass silicon is of increasing importance with the continuing technology scaling towards nano-sized devices.

3.2. RF front-ends for multistandard wireless receivers

Wideband LNAs covering a range from a few MHz to a up to several GHz should be investigated. Band selection in this case will rely on RF filters. Fully differential as well as single-ended designs are of interest, especially the latter which avoids off-chip baluns.

Narrow-band LNAs are also a viable solution covering the bands e.g. 900 MHz, 1800 and 1900 MHz, 2.4 GHz, and 5, 6 and 7 GHz including bias and device sizes optimisation techniques. Concurrent LNAs (LNAs with the ability to simultaneously receive signals at different bands) are of special interest. This will allow instances at the system level, when two standards are activated and are being processed in the same time, e.g. when a desktop is connected via e.g. 5 GHz WLAN to the Ethernet and in the same time to a keyboard or a printer via WPAN (Bluetooth).

High-Q inductors using reverse interconnect scaling topologies are critical components and new LNA topologies suitable for low-voltage operation should be explored. Innovative architecture-level design approaches is needed for both types of LNAs mentioned above in order to provide high-performing low-voltage operation.

Receiver architectures to accommodate concurrent further processing of signals should be explored together with work done in the spirit of the previous thrust. Techniques to digitally control gain and linearity as well as methods to control the amount of loss associated with inductive loads and tanks allowing fine and coarse control of the band selectivity are of special interest.

3.3. Techniques for robust physical design

While multistandard design and power optimisation techniques are considered, due importance must be attached to the development of highly robust design. Robustness aims at first-pass design success. Techniques developed to achieve such an objective maximise yield during manufacturing. Design centering techniques can subsequently make the design more robust against drift, aging and varying operating conditions (such as supply voltage variations), ensuring long-lasting and reliable performance.

Furthermore, one key performance limiting factor will be interference from other analog and digital circuits. Systematic robustness enhancements are achieved via circuit topologies, shielding and isolation techniques, and via frequency and timing planning.

Packaging trade-offs between on-chip versus off-chip solutions for multistandard come into consideration, in order to maximise the performance-to-cost ratio, see Ref. [8].

3.4. Programmable bandwidth frequency synthesisers

As mentioned before, multistandard RF transceivers combining several standards in one unit are of key importance. In reaching the ultimate goal of maximising the performance-to-cost ratio of such a module, careful studies on both the architectural design and the frequency planning is strongly required. One of the most challenging tasks is the implementation of a fully integrated high-performance frequency synthesiser using a standard CMOS process.

A solution for wideband frequency synthesis is to use PLL-based programmable frequency synthesisers, where the key circuit will be a GHz-range PLL used for frequency translation of the RF input signal. In part, this high-speed PLL consists of a low phase noise oscillator and a high-speed frequency divider. The development of these circuit blocks in CMOS, has been possible only recently with the emergence of submicron technologies. The other blocks within a PLL are the phase detector with charge pump, and a preferably passive loop filter. The advantages of digital technology should be invoked in order to achieve the high-performance goals.

However, the architecture described above would still require a very wideband RF VCO operation with low-power and low phase noise characteristics. So new VCO architectures will be looked for to satisfy the needs of such a system. Also hybrid fractional-N and integer-N synthesisers are of increasing importance in future designs.

3.5. Programmable and configurable baseband chains

Multistandard operation with different bandwidths, SNR and dynamic range requirements usually translates into a very wide range of specifications for analog baseband

components. While worst-case design approaches can allow components to be used for multistandard applications, power consumption and hardware requirements are not optimised. In order to develop a power-optimised multistandard baseband solution, circuit-level design techniques that optimise power and performance within individual filter and VGA sections should be developed. Specifically, techniques for DSP control of VGA gain and filter cutoff frequency must be investigated. At the architectural level, these optimised VGAs and filters will be used to develop a programmable, reconfigurable baseband chain with filter and amplifier sections. Configuration of this chain will be controlled by digital logic through an analog switch array. This baseband chain can potentially have the most significant contribution to the hardware saving for the entire receiver.

The rapid advancement in digital technology provides motivation for implementing all possible baseband blocks discussed above in the digital domain. This entails tradeoffs in the required linearity and power consumption between the filter, VGA and ADCs. The number of sections used depends mainly on the wireless standard under consideration as well as the available ADC resolution.

3.6. Programmable data converters for multistandard

The desire to realize an increasing portion of the receiver and transmitter functions in the digital domain increase both dynamic range and bandwidth required of ADCs. The urgent need is to develop techniques for high-resolution and wideband ADCs.

To allow multistandard operation, sigma-delta and pipelined converters are the most suitable candidates to meet the needs of large signal bandwidth and high dynamic range. Multibit sigma-delta ADC topologies combined with pipelined architectures are ideal for high-resolution wideband applications. Architectures which adopt standard pipeline ADCs and use sigma-delta modulation enhance linearity should be studied. Other important areas are topologies for high-order multibit delta-sigma modulators.

One important area is the trade-off between power consumption, resolution and bandwidth. For example the WCDMA standard requires a high-speed medium resolution converter while GSM requires a high resolution and medium speed converter. For WLAN even higher converter speeds than for WCDMA are needed. To design a low-power multi-standard ADC's with as much common hardware as possible is not a trivial task.

4. CONCLUSIONS

In order to realize the concept of SDR a lot of improvements have already been made in the digital domain, using general purpose and special purpose DSPs and ASICs. This trend will be further enhanced by the continuing device size shrinking, up to now following Moore's law.

However, the situation is completely different for analog, mixed-signal and RF designs. The analog performance do not improve with technology scaling. In fact the performance will deteriorate, and the components available for analog parts will be more and more non-ideal. Random variations will increase, forcing future analog designers to design with mainly statistical methods. In order to achieve the goal of first-pass designs this area of designing SoCs will increase in importance.

In view the conditions above, innovative solutions in the new down-sized technologies are necessary. Here CMOS will a dominating technology. An advantage with the scaling is, however, that the necessary digital correction and calibration circuitry will be almost "for free" since these parts will be small compared to the whole chip area.

The presentation at the conference will show more examples of the ideas presented in this paper.

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